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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,415	02/19/2002	James Aweya	57983.000061	2130

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,415	AWEYA ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/31/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ruffini (US Patent no 6,532,274 B1).

4. As per claim 1, Ruffini teaches

receiving a first timestamp and a second timestamp [Fig. 1; col. 13, lines 29-33; col. 20, lines 27-31; an element 2 having a local oscillator receives a first time stamp and a second time stamp transmitted by a main unit 1 that includes a transmitting unit to transmit a time stamp generated by a time generating unit at a predefined time intervals];

measuring a first time interval between the first timestamp and the second timestamp [col. 13, lines 57-65; col. 20, lines 32-47; variation in the arrival times of the time stamps];

generating a difference signal representing a difference between the first time interval and a second time interval [col. 13, lines 57-65; col. 20, lines 45-53; variations are time errors that constitutes the difference between pre-defined time intervals, and therewith expected, time interval between the time stamps and the actual time interval between received time stamps, wherein the local oscillator is adapted to measure this actual time interval]; and

generating a second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal [col. 13, lines 27-28, 57-65; col. 20, lines 25-26, 38-44; the calibrating unit is adapted to calibrate the local oscillator with the aid of the inter-arrival time of the time stamps].

5. As per claim 2, Ruffini teaches that generating a third timestamp and a fourth timestamp each indicating a respective time instance as determined by the second clock signal [Fig. 1; col. 13, lines 29-33; col. 20, lines 27-31; a main unit 1 that includes a transmitting unit to transmit a time stamp generated by a time generating unit at a predefined time intervals].

6. As per claim 3, Ruffini teaches that measuring the second time interval between the third timestamp and the fourth timestamp [col. 13, lines 57-65; col. 20, lines 32-47; variation in the arrival times of the time stamps].

7. As per claim 4, Ruffini teaches that the first timestamp and the third timestamp are each generated at a first discrete time instant, and the second timestamp and the fourth timestamp are each generated at a second discrete time instant [col. 13, lines 29-33].

8. As per claim 5, Ruffini teaches that initializing the difference signal prior to receiving the first timestamp and the second timestamp [inherent to the system].

9. As per claim 6, Ruffini teaches that filtering the difference signal such that the second clock signal is synchronized with the first clock signal based upon a filtered difference signal [inherent to the system as the calibrating unit is adapted to calibrate the local oscillator be synchronized with the main clock].

10. As per claim 7, Ruffini teaches that initializing the filtered difference signal prior to receiving the first timestamp and the second timestamp [inherent to the system].

11. As per claim 8, Ruffini teaches that controlling the period of a digitally controlled oscillator based upon the difference signal [col. 13, lines 27-28; a local oscillator; col. 15, lines 61-65; the local oscillator may be a voltage-controlled oscillator].

12. As per claim 9, Ruffini teaches that converting the difference signal from a digital difference signal value into analog difference signal value [inherent to the system; col. 15, lines 61-65]; and controlling the period of a voltage controlled oscillator based upon the analog difference signal value [col. 15, lines 61-65].

13. As per claim 10, Ruffini teaches that a computer signal embodied in a carrier wave readable by a computing system and encoding a computer program of instructions for executing a computer process performing the method recited in claim 1 [inherent to the system].

14. As per claim 20, Ruffini teaches an article of manufacture for synchronizing clocks in a network [Fig. 1; inherent as the invention is directed towards clocks synchronization in a network], the article of manufacture comprising:

at least one processor readable carrier [Fig. 1; inherent to the system as it is implemented in a network comprising a main unit and several nodes]; and

instructions carried on the at least one carrier [Fig. 1; inherent to the system as it is implemented in a network comprising a main unit and several nodes];

wherein the instructions are configured to be readable from the at least one carrier by at least one processor and thereby cause the at least one processor to operate so as to:

receive a first timestamp and a second timestamp [Fig. 1; col. 13, lines 29-33; col. 20, lines 27-31; an element 2 having a local oscillator receives a first time stamp and a second time stamp transmitted by a main unit 1 that includes a transmitting unit to transmit a time stamp generated by a time generating unit at a predefined time intervals];

measure a first time interval between the first timestamp and the second timestamp [col. 13, lines 57-65; col. 20, lines 32-47; variation in the arrival times of the time stamps];

generate a difference signal representing a difference between the first time interval and a second time interval [col. 13, lines 57-65; col. 20, lines 45-53; variations are time errors that constitutes the difference between pre-defined time intervals, and therewith expected, time interval between the time stamps and the actual time interval between received time stamps, wherein the local oscillator is adapted to measure this actual time interval]; and

generate a second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal [col. 13, lines 27-28, 57-65; col. 20, lines 25-26, 38-44; the calibrating unit is adapted to calibrate the local oscillator with the aid of the inter-arrival time of the time stamps].

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruffini (US Patent no 6,532,274 B1) in view of Rokugo (US Patent no 5,864,248).

17. As per claim 11, Ruffini discloses

a receiver for receiving a first timestamp and a second timestamp [Fig. 1; col. 13, lines 29-33; col. 20, lines 27-31; an element 2 having a local oscillator receives a first time stamp and a second time stamp transmitted by a main unit 1 that includes a transmitting unit to transmit a time stamp generated by a time generating unit at a predefined time intervals]; and

a first differencing element for measuring a first time interval between the first timestamp and the second timestamp [col. 13, lines 57-65; col. 20, lines 32-47; variation in the arrival times of the time stamps];

a second differencing element for generating a difference signal representing a difference between the first time interval and a second time interval [col. 13, lines 57-65; col. 20, lines 45-53; variations are time errors that constitutes the difference between pre-defined time intervals,

and therewith expected, time interval between the time stamps and the actual time interval between received time stamps, wherein the local oscillator is adapted to measure this actual time interval]; and

a variable oscillator for generating a second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal [col. 13, lines 27-28, 57-65; col. 20, lines 25-26, 38-44; the calibrating unit is adapted to calibrate the local oscillator with the aid of the inter-arrival time of the time stamps].

Ruffini does not expressly disclose about a phase-locked loop (PLL) associated within the receiver. But a routineer would know that it is well known in the art to utilize a phase-locked loop in a clock synchronization system. However, Rokugo expressly discloses the use of a phase-locked loop circuit in a receiver to reproduce clock signals synchronized with a transmitter in a communication system [Fig. 1 and 3; col. 1, lines 9-14; col. 2, line 54 -- col. 3, line 7]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to clock synchronization between transmitter and receiver circuits in a communication network system. Moreover, a routineer would like to use the phase-locked loop disclosed by Rokugo as it is highly stable against amplitude jitters [col. 8, lines 37-41]. Plus, with use of this PLL, a clock can be reproduced accurately and stably [col. 8, lines 52-55] and this PLL circuit can be implemented by a relatively simple circuit configuration [col. 8, lines 61-62].

18. As per claim 12, Ruffini discloses a pulse counter for generating a third timestamp and a fourth timestamp each indicating a respective time instance as determined by the second clock signal [Fig. 1; col. 13, lines 29-33; col. 20, lines 27-31; a main unit 1 that includes a transmitting unit to transmit a time stamp generated by a time generating unit at a predefined time intervals].

19. As per claim 13, Ruffini discloses a third differencing element for measuring the second time interval between the third timestamp and the fourth timestamp [col. 13, lines 57-65; col. 20, lines 32-47; variation in the arrival times of the time stamps].

20. As per claim 14, Ruffini discloses that the first timestamp and the third timestamp are each generated at a first discrete time instant, and the second timestamp and the fourth timestamp are each generated at a second discrete time instant [col. 13, lines 29-33].

21. As per claim 15, Ruffini discloses that the second differencing element initializes the difference signal prior to receiving the first timestamp and the second timestamp [inherent to the system].

22. As per claim 16, Rokugo discloses that a loop filter for filtering the difference signal such that the second clock signal is synchronized with the first clock signal based upon a filtered difference signal [Fig. 3].

23. As per claim 17, Rokugo discloses that the loop filter initializes the filtered difference signal prior to receiving the first timestamp and the second timestamp [inherent to the system].

24. As per claim 18, Ruffini discloses that the variable oscillator is a digitally controlled oscillator the period of which is controlled based upon the difference signal [col. 13, lines 27-28; a local oscillator; col. 15, lines 61-65; the local oscillator may be a voltage-controlled oscillator].

25. As per claim 19, Ruffini discloses that a digital-to-analog converter for converting the difference signal from a digital difference signal value into analog difference signal value, and wherein the variable oscillator is a voltage controlled oscillator the period of which is controlled based upon the analog difference signal value [inherent to the system; col. 15, lines 61-65].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
December 20, 2004

/THOMAS LEE
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